AMENDMENTS TO THE CLAIMS of SN 09/642,858

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1. (Original) A fuse-controlled error-correction control system for a ROM, comprising:

a defective memory-cell address detector circuit (CMP) that compares input address signals for the ROM to a fuse-controlled preset static address of a predetermined defective memory cell of the ROM and that provides an address-hit output signal (ADDHIT), which indicates the occurrence of input address signals corresponding to said fuse-controlled preset static address of said predetermined defective memory cell;

an (AOUT) circuit that receives the address-hit output signal ADDHIT signal and that provides a corresponding bit-reversal output signal (REV); and

a data output buffer that receives data bits from memory cells of the ROM, including a bit from said predetermined defective memory cell, and that has an output terminal coupled to a data output terminal of the ROM, said data output buffer having an output-reversal control terminal for receiving the bit-reversal output signal REV, which reverses the sense of the data signal corresponding to the predetermined defective memory cell at the output terminal of the data output buffer when the address of the defective memory cell is detected by the defective memory-cell address detector circuit CMP.

2. (Original) The fuse-controlled error-correction control system of Claim 1 wherein the defective memory cell address detector circuit CMP includes a comparator circuit that compares each bit of a multi-bit memory address signal to respective fuse-controlled static bits in an array of fused circuits that statically represent an address of the predetermined defective memory cell.

3. (Original) The fuse-controlled error-correction control system of Claim 2 wherein the comparator circuit uses exclusive logic (ADDXNOR) to compare individual bits of the multi-bit memory address signals to respective fuse-controlled static bits that represent an address of a defective memory cell.

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4. (Original) The fuse-controlled error-correction control system of Claim 2 wherein the fuse-controlled static bits for the address for the defective memory cell are provided by an array of fuses that are adapted to be blown by a laser beam.

5. (Original) The fuse-controlled error-correction control system of Claim 1

wherein the ROM includes a plurality of data output buffers; and

wherein the (AOUT) circuit that receives the address-hit output signal ADDHIT signal and that provides a corresponding bit-reversal output signal (REV) includes a fuse-controlled error-correction control system for selecting a particular one of said plurality of data output buffers.

6. (Original) The fuse-controlled error-correction control system of claim 1 including a circuit for recognizing an all 1's input address signal as an address for a defective memory cell.

7. (Original) The fuse-controlled error-correction control system of Claim 1 including an other defective memory-cell address detector circuit that compares input address signals for the ROM to an other fuse-controlled preset static address of an other predetermined defective memory cell of the ROM and that provides an other address-hit output signal (ADDHIT), which indicates the occurrence of the other input address signals corresponding to said fuse-controlled preset static address of said other predetermined defective memory cell.

8. (Original) A fuse-controlled error-correction control system for a ROM, comprising:

a defective memory-cell address detector circuit (CMP) that compares input address signals for the ROM to a plurality of fuse-controlled preset static addresses of a predetermined corresponding plurality of defective memory cells of the ROM and that provides a plurality of corresponding address-hit output signals (ADDHIT), which indicate the occurrence of one of the input address signals corresponding to one of the fuse-controlled preset static addresses of one of the predetermined defective memory cells;

an (AOUT) circuit that receives the address-hit output signals ADDHIT signal and that provides a corresponding bit-reversal output signal (REV)for each defective memory cell; and

a plurality of data output buffers that receives data bits from memory cells of the ROM, including bits from said predetermined defective memory cells, each of said plurality of data output buffers having an output terminal coupled to a data output terminal of the ROM, each of said data output buffers having an output-reversal control terminal for receiving one of the bit-reversal output signals REV that reverses the sense of the data signal corresponding to one of the predetermined defective memory cell at the output terminal of the data output buffer when the address of one of the defective memory cell is detected by the defective memory-cell address detector circuit CMP.

9. (Original) The fuse-controlled error-correction control system of Claim 8 wherein the defective memory cell address detector circuit CMP includes a plurality of comparator circuits that compares each bit of a multi-bit memory address signal to respective fuse-controlled static bits in an array of fused circuits that statically represent addresses of the predetermined defective memory cells.

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~~10~~. (Currently Amended) The fuse-controlled error-correction control system of Claim ~~7~~ 8. wherein the comparator circuit uses exclusive logic (ADDXNOR) to compare individual bits of the multi-bit memory address signals to respective fuse-controlled static bits that represent the address of the defective memory cells.

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~~11~~. (Original) The fuse-controlled error-correction control system of Claim 9 wherein the fuse-controlled static bits for the addresses for the defective memory cells are provided by an array of fuses that are adapted to be blown by a laser beam.

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12. (Currently Amended) The fuse-controlled error-correction control system of Claim ~~1~~ 8

wherein the ROM includes a plurality of data output buffers; and

wherein the (AOUT) circuit that receives the address-hit output signal ADDHIT signals and that provides corresponding bit-reversal output signals (REV) includes a fuse-controlled error-correction control system for selecting a particular one of said plurality of data output buffers.

13. (Original) A method of controlling error-correction for a ROM, comprising the steps of:

comparing input address signals for the ROM to a fuse-controlled preset static address of a predetermined defective memory cell of the ROM;

providing an address-hit output signal (ADDHIT), which indicates the occurrence of input address signals corresponding to said fuse-controlled preset static address of said predetermined defective memory cell;

providing a corresponding bit-reversal output signal (REV) in response to the address-hit output signal ADDHIT;

in response to the bit-reversal output signal (REV), reversing the sense of the data signal corresponding to the predetermined defective memory cell at the output terminal of a data output buffer when the address of the defective memory cell is detected by the defective memory-cell address detector circuit CMP.

14. (Currently Amended) The method of Claim ~~14~~ 13 wherein the step of comparing input address signals for the ROM to a fuse-controlled preset static address of a predetermined defective memory cell of the ROM includes comparing each bit of a multi-bit memory address signal to respective fuse-controlled static bits in an array of fused circuits that statically represent an address of the predetermined defective memory cell.

15. (Original) The method of Claim 14 wherein the step comparing includes using exclusive logic (ADDXNOR) to compare individual bits of the multi-bit memory address signals to respective fuse-controlled static bits that represent an address of a defective memory cell.

16. (Original) The method of Claim 14 wherein the step of comparing includes providing the fuse-controlled static bits for the address for the defective memory cell with an array of fuses that are adapted to be blown by a laser beam.

17. (Original) The method of Claim 13 includes providing a plurality of data output buffers; and selecting a particular one of said plurality of data output buffers for receiving the address-hit output signal ADDHIT signal that provides a corresponding bit-reversal output signal (REV) includes controlling said selection with a fuse-controlled error-correction control system.

18. (Original) The method of Claim 13 including the step of recognizing an all 1's input address signal as an address for a defective memory cell.

19. (Original) The method of Claim 13 including

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comparing input address signals for the ROM to an other fuse-controlled preset static address of an other predetermined defective memory cell of the ROM; and

providing an other address-hit output signal (ADDHIT), which indicates the occurrence of the other input address signals corresponding to said fuse-controlled preset static address of said other predetermined defective memory cell.